REMARKS

This responds to the Office Action mailed on January 31, 2006, and the references cited therewith.

Claims 1, 2, 5, 28 and 29 are amended, no claims are canceled, and no claims are added; as a result, claims 1-8, 28 and 29 remain pending in this application.

Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a), stating that the "two or more memory sections" and the "each memory section includes two or more TLBs"be shown or that the features be canceled from the claims.

Applicant respectfully submits that no drawing corrections are needed. Applicant directs the Examiner's attention to the two or more memory sections 130 shown in Fig. 1 and described at p. 5, lines 3-5. The plurality of TLBs within each memory section 130 is shown in Figs. 2 and 3 and described at p. 5, line 20 through p. 6, line 24.

Claim Objections

Claims 3 & 28 and 4 & 29 were objected to under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claims 28 and 29 have been amended to make them dependent on claim 8.

Claims 5-8 were objected to as containing subject matter which was not described in the specification at the time the application was filed. In particular, the Examiner stated that it appears that the limitations added to claims 5-8 of "two or more memory sections" and "each memory section includes two or more TLBs" were not described in the specification at the time the application was filed.

Applicant directs the Examiner's attention to the two or more memory sections 130 shown in Fig. 1 and described at p. 5, lines 3-5. The plurality of TLBs within each memory section 130 is shown in Figs. 2 and 3 and described at p. 5, line 20 through p. 6, line 24.

§102 Rejection of the Claims

Claims 8 and 1 were rejected under 35 U.S.C. § 102(b) for anticipation by Teller et al. ("Locating Multiprocessor TLBs at Memory", *Proceedings of the twenty-Seventh Annual Hawaii International Conference on System Science*, 1994, pp. 554-563).

Teller describes memory-based TLBs. Teller's TLBs are located at each memory module. They receive a virtual address from a processor and generate a physical address on the memory module associated with the virtual address. Each of Teller's TLBs is capable of receiving a memory request from each processor in the system. Therefore, Teller must provide a complex page table snooping methodology such as what is detailed in Teller at p. 557, col.1, lines 10-14.

Applicant, on the other hand, describes a memory system having two or more sections. Each section includes two or more TLBs. A memory request from a processor which is routed to one of the memory sections is routed to a TLB associated with the requesting processor. That TLB then translates the address received from the processor into a physical memory address within the memory section. Claims 1 and 2 have been amended to more clearly point out this difference. Claim 8 already makes this distinction.

The Examiner seemed to state that Teller includes mapping means having a first TLB for a first processor and a second TLB for a second processor. Applicant is unable to see in Teller any teaching or suggestion for associating a particular TLB with a particular processor. In fact, Teller teaches away from that approach by requiring that each TLB be capable of receiving memory requests from any of the processors. Reconsideration and allowance of claims 1-8, 28 and 29 is respectfully requested.

§103 Rejection of the Claims

Claims 4 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Teller et al. in view of Peck, Jr. et al. (US 6,686,920).

The Examiner stated that although Teller does not specifically disclose an I/O processor and its associated I/O TLB, such a construct is described in Peck.

Applicant respectfully submits that Peck teaches a processor-based TLB while Teller teaches a memory-based TLB. There is no teaching or suggestion in either reference for placing a TLB associated with an I/O device within memory, as described by Applicant and claimed in claims 4 and 29. Reconsideration of claims 4 and 29 is respectfully requested.

Claims 2, 3 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Teller et al. in view of Herrell et al. (US 5,310,287).

The Examiner stated that although Teller does not specifically disclose placing a FIFO at the memory interface, Heller does disclose such a FIFO. The section in Heller describes a FIFO within a DMA engine that is separate from physical memory. In fact, the approach used by Heller would be similar to placing a FIFO in the I/O device 190 described by Applicant. Reconsideration of claims 2, 3, and 28 is respectfully requested.

Allowable Subject Matter

Claims 5-7 were indicated to be allowable if rewritten to overcome the claim objections. Applicant respectfully submits that the objections have been addressed and overcome above. No claim amendments are necessary.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date July 31, 2006

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31st day of JULY ~~March~~ 2006.

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Signature